**CMPEN 371: Advanced Digital Design**

**Fall 2015**

**Lab 2: Basic Combinational Components**

**Due: 9 September 2015**

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**ACKNOWLEDGEMENT**

This work is entirely our own and I did not provide any assistance except as noted. The approximate contribution of each team member is as follows:

50% Kevin Brenneman \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

50% Richard Lucas \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Grading Rubric**

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| **Criteria** | **Grade** |
| Design (Sound algorithm, good block diagrams / state diagrams / state tables, efficient design, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Translate to VHDL (VHDL matches design docs, good comments / whitespace, follows guidelines, efficient coding, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Test in Simulator (test bench or script for each component and FSM, good coverage, components / FSMs verified, etc.)  Excellent: 3; Good: 2; Satisfactory: 1; Unsatisfactory: 0; Failure: -1 or worse | / 3 |
| Test in Hardware (demo in lab)   * Switches enter A and B, Sum and overflow displayed properly on LEDs * Subtract works * Buttons select A, B or Sum for 7-segment display properly * 7-segment digits are correct * Other | / 35 |
| Bonus (optional challenge, etc.) |  |
| Penalty (late demo, late submission on ANGEL, team member absent from demo, etc.)  Demo late in lab: -2; Demo up to 5 days late: -5; Demo more than 5 days late: -10  Submitted late or incompletely on ANGEL: -5; Not submitted on ANGEL: no grade for lab |  |
| TOTAL | / 50 |

**DESIGN**

The following design documents are attached:

Filename Description

351\_lab02\_block diagram.pdf top level diagram showing how everything is connected. all internal components are simple or have been covered in detail in a previous lab.

**TRANSLATE TO VHDL**

The following HDL models are attached:

Filename Description

lab02\_kjb5568\_rjl5336 Top Level: Links together lab 1 with a mux, some combinational logic, and a hex to seven segment display allowing us to display on the seven segment display

Mux4to1.vhd Component: 4:1 mux that has a 4 bit output. uses a select statement for logic

hextosevenseg.vhd Component: converts 4 bit hex that allows us to send it to a single seven segment display. uses a when else statement for logic

The following HDL models and other files are not attached but are submitted electronically:

Filename Description

rippe\_carry\_adder.vhd component: 4 bit adder used in lab 1

AdderSubtractor\_4bit.vhd component: top level of lab 1. adds or subtracts two 4 bit 2's complement numbers with the ability to show overflow

fulladder.vhd component: 2 bit adder that is used in the rca

**TEST IN SIMULATOR**

The following files were used for testing to verify the design:

Filename Description

toplevel\_tb a non exhaustive test bench was used, bits of each possible scenario were tested. all tests passed so further exhaustive testing was not required

Mux4to1\_tb.vhd an exhaustive test bench was used as there were only 4 possible cases here. all test passed

hextosevenseg\_tb.vhd an exhaustive test bench was provided and all tests passed.

**TEST IN HARDWARE**

Full functionality was achieved in hardware.

**PERFORMANCE**

The following cost and performance metrics were obtained:

Area (resources used)

Number of Slice Registers: 00

Number of Slice LUTs: 12

**QUESTIONS**

No questions to answer.